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10/630,994	07/30/2003	Ken Gary Pomaranski	200311225-1	7732

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EXAMINER	
SAVLA, ARPAN P	

ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 11/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/630,994	POMARANSKI ET AL.	
	Examiner	Art Unit	
	Arpan P. Savla	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 July 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/30/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The instant application having Application No. 10/630944 has a total of 18 claims pending in the application, there are 4 independent claims and 14 dependent claims, all of which are ready for examination by Examiner.

INFORMATION CONCERNING OATH/DECLARATION

Oath/Declaration

1. Applicant's oath/declaration has been reviewed by Examiner and is found to conform to the requirements prescribed in 37 CFR 1.63.

STATUS OF CLAIM FOR PRIORITY IN THE APPLICATION

2. Acknowledgment is made that Applicant is not claiming any priority for the filing date of the application.

INFORMATION CONCERNING DRAWINGS

Drawings

3. Applicant's drawings submitted July 30, 2003 are acceptable for examination purposes.

ACKNOWLEDGMENT OF REFERENCES CITED BY APPLICANT

Information Disclosure Statement

4. As required by MPEP § 609(c), Applicant's submission of the Information Disclosure Statement dated July 30, 2003 is acknowledged by Examiner and cited references have been considered in the examination of the claims now pending. As required by MPEP § 609 c(2), a copy of the PTOL-1449 initialed and dated by the examiner is attached to the instant office action.

OBJECTIONS

Specification

5. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The following title is suggested: "Persistent Volatile Memory Fault Tracking Using Entries In The Non-Volatile Memory Of A Fault Storage Unit."

6. The disclosure is objected to because it contains an embedded hyperlink and/or other form of browser-executable code on page 7, line 22. Applicant is required to delete the embedded hyperlink and/or other form of browser-executable code. See MPEP § 608.01.

7. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: The phrase "logical analysis" is used in claim 4, however, it is not located anywhere within the specification. Thus, there is no clear description as to what this "logical analysis" entails.

Appropriate correction is required.

Claims

8. Claims 1-2, 7, and 15 are objected to because of the following informalities:

9. **As per claim 1**, the phrase "an fault storage unit" in line 6 should be "a fault storage unit".

10. **As per claim 2**, it is unknown whether the phrase "the particular memory module" in line 1 is referring to "that particular memory module" in line 6 of claim 1 or another particular memory module.

11. **As per claim 7**, it is unknown whether phrase "the particular memory module" in 3 is referring to "that particular memory module" in line 6 of claim 1 or another particular memory module.

12. **As per claim 15**, the claim recites the limitation "the entries" in lines 2 and 3. There is insufficient antecedent basis for this limitation in the claim. Applicant may consider amending this claim to read "entries" in line 2 and "said entries" in line 3.

Appropriate corrections are required.

REJECTIONS NOT BASED ON PRIOR ART

Claim Rejections - 35 USC § 112

13. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

14. **Claim 4 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement.** The claim contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The subject matter in question is "logical analysis" in line 2. The phrase "logical analysis" is not located anywhere within the specification. Thus, there is no clear description as to what this "logical analysis" entails. Examiner will interpret that logical analysis refers to a modulation analysis of a historical list of fault weights throughout the rest of this instant office action.

15. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

16. **Claim 12 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention.** The phrase "configured to connect to" in line 2 does not clearly identify if the connector is actually connected to anything or not.

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 102

17. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

18. Claims 1-3, 6-7 are rejected under U.S.C. 102(b) as being anticipated by Jeddeloh et al. (U.S. Patent 5,862,314), hereafter "Jeddeloh-314".

19. **As per claim 1**, Jeddeloh-314 discloses a method for persistently tracking volatile memory faults, the method comprising:

detecting a memory error relating to at least one dynamic random access memory (DRAM) unit on a particular memory module (col. 2, lines 51-55; col. 3, lines 3-12; and Fig. 2 element 50); It should be noted that the error detecting occurs when the "error map" is being created in the factory that makes the memory module.

and writing an entry pertaining to the memory error in non-volatile memory of an fault storage unit on that particular memory module (col. 2, lines 59-65; col. 3, lines 3-6; and Fig. 2, elements 52 and 54). It should be noted that the "error map" is analogous to the "fault storage unit".

20. **As per claim 2**, Jeddeloh-314 discloses the particular memory module comprises a particular dual in-line memory module (DIMM) of a plurality of DIMMs in a memory system (col. 2, lines 49-51 and Fig. 1, element 12).

21. **As per claim 3**, Jeddeloh-314 discloses determining a scope of the detected memory error (col. 3, lines 38-47). It should be noted that when taking the broadest interpretation of the claim language it is clear that the limitations of the claim do not specify what determines the specific scope of the detected memory error. Jeddeloh-314 assigns error tags to defective memory portions, thus determining a scope of the detected memory error.

22. **As per claim 6**, Jeddeloh-314 discloses reading the entry from the non-volatile memory of the fault storage unit (col. 3, lines 27-30 and Fig. 2, element 56); It should be noted that when "the processor in the memory controller receives a copy of the error map" it is analogous to "reading the entry from the non-volatile memory of the fault storage unit".

and removing memory bits associated with the memory error from a set of usable memory (col. 3, lines 52-63 and Fig. 2, element 60). It should be noted that remapping error bits is virtually removing bits from defective portions of memory by re-addressing the bits to working portions of memory, thus, removing the entire portion of defective memory as far as the system processor is concerned.

23. **As per claim 7**, Jeddeloh-314 discloses removing memory bits associated with the memory error from a set of usable memory while the particular memory module remains online (col. 3, lines 52-63; col. 4, lines 49-57; and Fig. 2, element 60). It should be noted that since the creating and storing of the remapping table is transparent to the processor, the memory module continues to stay online while the error bits are remapped. Also, see citation note for claim 6 above in regards to remapping error bits.

24. Claims 8, 11, and 18 are rejected under U.S.C. 102(b) as being anticipated by Jeddeloh et al. (U.S. Patent 6,052,798), hereafter "Jeddeloh-798".

25. **As per claim 8**, Jeddeloh-798 discloses a memory module that persistently tracks volatile memory faults, the memory module comprising:

a plurality of dynamic random access memories (DRAMs) (col. 3, lines 61-63 and Fig. 1, element 12);

and a fault storage unit including non-volatile memory configured to store entries pertaining to faults in the plurality of DRAMs on that memory module (col. 2, line 59 – col. 3, line 6 and Fig. 1, elements 16 and 18). See citation note for claim 1 above.

26. **As per claim 11**, Jeddeloh-798 discloses the memory module comprises a dual in-line memory module (DIMM) (col. 2, lines 57-59 and Fig. 1, element 12).

27. **As per claim 18**, Jeddeloh-798 discloses a memory system comprising:

means for reading data from and writing data to volatile memory units on a plurality of memory modules (col. 4, lines 26-34; col. 5, lines 53-59; and Fig. 1, element 20); It should be noted that page 7, lines 5-6 of Applicant's specification defines means as a memory controller.

and means for reading error entries from and writing error entries to a non-volatile fault storage unit on each memory module (col. 3, lines 36-39 and Fig. 1, element 36). It should be noted that page 8, lines 13-15 of Applicant's specification defines means as a memory error interface.

Claim Rejections - 35 USC § 103

28. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

29. Claim 4 is rejected under 35 U.S.C. 103(a) as being obvious over Jeddeloh-314 in view of Abel et al. (U.S. Patent 4,633,467).

30. Jeddeloh-314 discloses the method of claim 1.

Jeddeloh-314 does not expressly disclose the scope of the memory error is determined by a logical analysis of a history of faults associated with the particular memory module.

Abel discloses the scope of the memory error is determined by a logical analysis of a history of faults associated with the particular memory module (col.1, lines 52-55; col. 3, lines 18-34; col. 4, lines 53-68; and col. 5, lines 21-41). It should be noted that Abel's "logical analysis" is a modulation analysis of a historical list of fault weights.

Jeddeloh-314 and Abel are analogous art because they are from the same field of endeavor, that being fault detection in computer units.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use Abel's modulation analysis of a historical list of fault weights on Jeddeloh-314's error map for identifying defective memory.

The motivation for doing so would have been to achieve system redundancy and automatic detection of system malfunctions to enhance system reliability (Abel, col. 1, lines 18-21).

Therefore, it would have been obvious to combine Abel with Jeddeloh-314 for the benefit of obtaining the invention as specified in claim 4.

31. Claim 5 is rejected under 35 U.S.C. 103(a) as being obvious over Jeddeloh-314 in view of Raynham et al. (U.S. Patent 5,774,647).

32. Jeddeloh-314 discloses the method of claim 1.

Jeddeloh-314 does not expressly disclose the entry comprises a DRAM unit identifier, a low bit number of a range, a high bit number of the range, and tag bits indicating time of last failure and number of occurrences of failure.

Raynham discloses the entry comprises a DRAM unit identifier, a low bit number of a range, a high bit number of the range, and tag bits indicating time of last failure and number of occurrences of failure (col. 9, lines 5-7; col. 10, lines 8-13 and 33-35; and col. 7, Table 2, the contents of bytes 24, 27, 41, 42, 54, and 118). It should be noted that when taking the broadest interpretation of the claim language it is clear that the limitations of the claim do not identify what specific range the low bit and high bit entail. Raynham discloses a time stamp indicating when the DIMM was turned on, thus the time stamp entails a time range and includes a low bit of the time range and also a high bit of the time range. It should also be noted that byte 41 in Table 2 is analogous to the "DRAM unit identifier".

Jeddeloh-314 and Raynham are analogous art because they are from the same field of endeavor, that being logging errors in the non-volatile memory of memory modules.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Raynham's specific error log bytes with Jeddeloh-314's entry on the non-volatile fault storage unit.

The motivation for doing so would have been to have management data containing identifying information about the DIMM, thus providing an efficient way to

manage memory modules in a computer system (Raynham, col. 2, lines 32-33 and col. 7, lines 62-64).

Therefore, it would have been obvious to combine Raynham with Jeddeloh-314 for the benefit of obtaining the invention in claim 5.

33. Claim 10 is rejected under 35 U.S.C. 103(a) as being obvious over Jeddeloh-798 in view of Bowden et al. (U.S. Patent 4,964,129).

34. Jeddeloh-798 discloses an entry stored in the non-volatile memory of the fault storage unit (col. 3, lines 3-6 and Fig. 1, element 18).

Jeddeloh-798 does not disclose expressly an entry that includes a DRAM identifier and a range of bits.

Bowden discloses an entry that includes a DRAM identifier and a range of bits (col. 6, lines 2-5). It should be noted that when taking the broadest interpretation of the claim language it is clear that the limitations of the claim do not identify what the "range of bits" specifically entails. Bowden discloses 4 memory row selects. These memory row selects are innately a range of bits.

Jeddeloh-798 and Bowden are analogous art because they are from the same field of endeavor, that being logging DRAM errors.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Bowden's specific error log entry with Jeddeloh-798's entry on the non-volatile fault storage unit.

The motivation for doing so would have been to reduce factory replacement time since the problem chips are preidentifiable, thus eliminating further testing to locate defective chips (Bowden, col. 8, lines 42-44).

Therefore, it would have been obvious to combine Bowden with Jeddeloh-798 for the benefit of obtaining the invention in claim 10.

35. Claims 9, 12, and 17 are rejected under 35 U.S.C. 103(a) as being obvious over Jeddeloh-798 in view of Galanti (U.S. Patent 3,693,052).

36. **As per claim 9**, Jeddeloh-798 discloses interface circuitry configured to provide read and write access by a memory error interface unit to the non-volatile memory of the fault storage unit (col. 3, lines 36-39 and Fig. 1, elements 16 and 36). It should be noted that for there to be any connection between the memory error interface unit and the non-volatile memory of the fault storage unit (or any computer units in general) it is inherently required there be "interface circuitry". The bus line arrows between element 18 and element 20 in Fig. 1 are being citied even though they are not labeled as an element.

Jeddeloh-798 does not disclose expressly that the memory error interface unit is on a circuit board.

Galanti discloses a circuit board (col. 2, lines 45-46 and Fig. 1, element 10).

Jeddeloh-798 and Galanti are analogous art because they are from the same field of endeavor, that being electrical circuitry.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to lay Jeddeloh-798's memory error interface unit on Galanti's circuit board.

The motivation for doing so would have been to make it economically possible to mass produce electronic apparatuses, save space and weight, and substantially increase the reliability of electronic equipment (Galanti, col. 1, lines 22-26).

Therefore, it would have been obvious to combine Galanti with Jeddeloh-798 for the benefit of obtaining the invention as specified in claim 9.

37. **As per claim 12**, Jeddeloh-798 discloses a memory module which includes multiple volatile memory units and a non-volatile fault storage unit (col. 2, line 59 – col. 3, line 2 and Fig. 1, element 12);

a memory controller configured to read and write data into the volatile memory units of memory modules (col. 4, lines 26-34; col. 5, lines 53-59; and Fig. 1, element 20); and

a memory error interface configured to provide read and write access to the non-volatile fault storage units of the memory modules (col. 3, lines 36-39 and Fig. 1, element 36). It should be noted that the "processor in the memory controller" is analogous to the "memory error interface". Also, see citation note for claim 6 above in regards to read/write access to the non-volatile fault storage unit.

Jeddeloh-798 does not disclose expressly that the memory error interface is on a circuit board and also does not disclose expressly a plurality of connectors, each connector configured to connect to a memory module.

Galanti discloses a circuit board comprising a plurality of connectors, each configured to connect to a memory module (col. 2, lines 45-46 and 64-65; col. 3, lines 15-20; Fig. 1, elements 10 and 20). It should be noted that the phrase "leads" is analogous to "connectors".

Jeddeloh-798 and Galanti are analogous art because they are from the same field of endeavor, that being electrical circuitry.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to lay Jeddeloh-798's memory controller and memory error interface on Galanti's circuit board and configure Galanti's leads to connect to Jeddeloh-798's memory module.

The motivation for doing so would have been to make it economically possible to mass produce electronic apparatuses, save space and weight, and substantially increase the reliability of electronic equipment (Galanti, col. 1, lines 22-26).

Therefore, it would have been obvious to combine Galanti with Jeddeloh-798 for the benefit of obtaining the invention as specified in claim 12.

38. **As per claim 17**, Jeddeloh-798 discloses the volatile memory units comprise dynamic random access memory (col. 3, lines 61-63 and Fig. 1, element 12);

and wherein the plurality of memory modules comprise dual in-line memory modules (DIMMs) (col. 2, lines 57-59 and Fig. 1, element 12).

39. Claims 13-16 are rejected under 35 U.S.C. 103(a) as being obvious over Jeddeloh-798 in view of Galanti as applied to claim 12 above, and further in view of Cepulis et al. (U.S. Patent 6,496,945).

40. **As per claim 13**, Jeddeloh-798/Galanti discloses the circuit board of a system of claim 12. See citations for claim 12 above.

Jeddeloh-798/Galanti does not disclose expressly a processor dependent hardware interface communicatively coupled between a central processing unit and the memory error interface.

Cepulis discloses a processor dependent hardware interface communicatively coupled between a central processing unit and the memory error interface (col. 5, line 66 – col. 6, line 17; col. 6, lines 33-36 and 55-67; and Fig. 1, elements 102, 106, and 122). It should be noted that "BIOS ROM" is analogous to "processor dependent hardware" and that "memory controller" is analogous to "memory error interface". It should also be noted the path of communication in Cepulis's system. The CPU accesses the BIOS ROM through a BIOS call. The CPU is coupled to the North Bridge and the BIOS ROM is coupled to the South Bridge, so any BIOS call passes through both bridges. The once the BIOS ROM receives the instructions it forwards them to the memory controller which then performs the read/write functions on the memory module. So even though the BIOS ROM is not physically coupled between the CPU and memory controller, it is still communicatively coupled between the CPU and memory controller.

Jeddeloh-798/Galanti and Cepulis are analogous in the art because they are from the same field of endeavor, that being fault detection and logging using non-volatile memory.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to interface Cepulis's BIOS ROM with Jeddeloh-798/Galanti's memory module and circuit board containing a memory controller and memory error interface.

The motivation for doing so would have been to have the user not need to run a separate utility program after replacing a failed device, adding a new device, or logically or physically relocating a failed device within the computer system, thus alleviating the inconvenience problems associated with conventional computer systems (Cepulis, col. 10, lines 5-9).

Therefore, it would have been obvious to combine Cepulis with Jeddeloh-798/Galanti for the benefit of obtaining the invention as specified in claim 13.

41. **As per claim 14**, Cepulis discloses a processor dependent code (PDC) unit accessible via the PDH interface, wherein the PDC unit includes boot code and error handling code (col. 6, lines 55-59; col. 7, lines 1-4; and Fig. 1, element 122). It should be noted that "processor dependent code" is analogous to "firmware" with is also analogous to "BIOS code". It should also be noted that the "Power On Self Test (POST)", which is part of the BIOS code, is code to test the computer's hardware for errors, this same code being analogous to "error handling code".

42. **As per claim 15**, Jeddeloh-798 discloses a system to remove memory bits associated with the entries from a set of useable memory (col. 3, lines 52-63 and Fig. 2, element 60). See citation note from claim 6 above.

Cepulis discloses the boot code includes instructions to read the entries from the non-volatile fault storage unit (col. 9, lines 24-26 and Fig. 1, elements 132 and CPU0

(BSP)). It should be noted that the phrase "failure device log (FDL) stored in non-volatile memory" is analogous to "non-volatile fault storage unit". It should also be noted that the "BIOS code" contains "boot code" which is executed by the boot strap processor (BSP) in order to read an entry from the FDL.

43. **As per claim 16**, Cepulis discloses the error handling code includes instructions to write entries relating to detected memory errors into the non-volatile fault storage unit and to read said entries from the non-volatile fault storage unit (col. 2, lines 54-56; col. 3, lines 8-10; col. 8, lines 9-14; col. 9, lines 19-20; Fig. 1, elements 102, 130, and 132). See citation note for claim 15 above regarding the FDL. It should be noted that the "BIOS code" contains the "error handling code" which is executed by the CPU 102 in order to place an entry in the FDL.

Conclusion

STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by MPEP 707.70(i):

CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, claims 1-18 have received a first action on the merits and are subject of a first action non-final.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Arpan P. Savla whose telephone number is (571) 272-1077. The examiner can normally be reached on M-F 8:30-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Arpan Savla
Assistant Examiner
11/8/05

DONALD SPARKS
SUPERVISORY PATENT EXAMINER